R20 Regulation *Subject code: 3P6DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, April 2026

VLSI DESIGN

(ECE)

Maximum Marks: 70 Date: 21.04.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Define body effect.	2M	1	L1
2	Define figure of merit.	2M	1	L1
3	Explain different MOS layers.	2M	2	L1
4	Sketch a stick diagram for CMOS inverter.	2M	2	L1
5	Define switch logic.	2M	3	L1
6	What is fan-in of a gate?	2M	3	L1
7	Draw the circuit diagram of SRAM cell.	2M	4	L1
8	What is parity generator?	2M	4	L1
9	Draw the circuit of Half adder using PAL.	2M	5	L1
10	What are functionality tests?	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Use neat sketches and explain BICMOS fabrication in an n-well process.	10M	1	L2
	OR			
12	Illustrate the operation of NMOS enhancement transistor in detail.	10M	1	L2
13	Sketch the schematic, stick diagram and layout for the Boolean expression Y = (AB + C).	10M	2	L2
	OR			
14	a) Categorize and explain scalable design rules. b) Specify the reasons to follow design rules for layout design.	5M 5M	2	L2
15	Explain about alternate gate circuits.	10M	3	L2
	OR			
16	What are the issues involved in driving large capacitive loads in VLSI circuits? Elaborate.	10M	3	L2
17	Construct the basic circuit diagram of static RAM cell and explain its read and write operation.	10M	4	L2

	OR			
18	a) Analyze and design a four-bit parity generator using only XOR gates. b) Draw the circuit diagram of carry select adder and explain it.	5M 5M	4	L2
19	a) Compare various programmable devices. b) What are the factors that are influencing low power design.	5M 5M	5	L2
	OR			
20	Analyze and explain the need of chip testing and occurrence of testing a chip at different levels.	10M	5	L2